Attorney's Docket No. 9253-2

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re: Kantabutra et al.
Serial No.: 10/029,836
Filed: October 23, 2001
Confirmation No.: 5330
Group Art Unit: 2121
Examiner: Tan V. Mai

For: **ADDERS AND ADDER BIT BLOCKS HAVING AN INTERNAL PROPOGATION CHARACTERISTIC INDEPENDENT OF A CARRY INPUT TO THE BIT BLOCK AND METHODS FOR USIGN THE SAME**

December 11, 2002

Commissioner for Patents
Washington, DC 20231

INFORMATION DISCLOSURE STATEMENT

Sir:

Attached is a list of documents on form PTO-1449 together with a copy of each identified document. It is requested that these documents be considered by the Examiner and officially made of record in accordance with the provisions of 37 C.F.R. § 1.97 and Section 609 of the MPEP. The Commissioner is hereby authorized to charge any additional fee, which may be required, or credit any refund, to our Deposit Account No. 50-0220.

Respectfully submitted,

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Certificate of Mailing under 37 CFR 1.8

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, Washington, DC 20231, on December 11, 2002.

Signature: _____
Carey Gregory
Date of Signature: December 11, 2002

FORM PTO-1449 U.S. Department of Commerce Patent and Trademark Office LIST OF DOCUMENTS CITED BY APPLICANT (Use several sheets if necessary)	Attorney Docket Number 9253-2	Serial No. 10/029,836
	Applicants: Kantabutra et al.	
	Filing Date October 23, 2001	Group 2121

U. S. PATENT DOCUMENTS

Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date if Appropriate
	1	5,508,925	10/19/93				

FOREIGN PATENT DOCUMENTS

		Document Number	Date	Country	Class	Subclass	Translation Yes | No

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

	2	Koren, I.: "Computer Arithmetic Algorithms," Prentice-Hall, 1993; pp. 73-92.
	3	Kantabutra, V.: "Designing Optimum One-Level Carry-Skip Adders," IEEE Trans. on Comp., 1993, Vol. 42, n.6, pp. 759-764
	4	Chan, P.K., Schlag, M.D.F., Thomborson, C.D. Oklobdzija, V.G.: "Delay Optimization of Carry-Skip Adders and Block Carry-Look-Ahead Adders," Proc. of Int'l Symposium on Computer Arithmetic, 1991, pp. 154-164,
	5	Nagendra, C., Irwin, M.J., Owens, R.M.: "Area-Time-Power Tradeoffs in Parallel Adders," IEEE Trans. CAS-II, 43, (10), pp. 689-702
	6	T. Lynch, E.E. Swartzlander, "A spanning-tree carry-look-ahead adder," IEEE Trans. on Comp., Vol. 41, n.8, Aug. 1992
	7	Kantabutra, "A Recursive Carry-Look-Ahead/Carry-Select Hybrid Adder," IEEE Trans. on Comp., Vol. 42, n.12, Dec. 1993.
	8	R. Zimmermann and H. Kaeslin, "Cell-Based Multilevel Carry-Increment Adders with Minimal AT-and PT-Products, unpublished manuscript at http://www.iis.ee.ethz.ch/~zimmi/
	9	A. Tyagi, "A Reduced-Area Scheme for Carry-Select Adders," IEEE Trans. on Comp., Vol. 42, n.10, Oct. 1993
	10	P. Corsonello, S. Perri, and V. Kantabutra, "Design of 3:1 multiplexer standard cell", Electronics Letters, November 23, 2000, vol. 36, No. 24, pp. 1994-1995.

EXAMINER _____ DATE CONSIDERED

*EXAMINER Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.